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Third Semester B.E./B.Tech. Degree Examination, June/July 2025

Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. Explain voltage divider bias circuit with a neat diagram and necessary derivations. (08 Marks)
- b. Explain inverting Schmitt Trigger with a neat diagram and waveform. (06 Marks)
- c. The base bias circuit shown in the Fig Q1(c), for the values indicated calculate I_B , I_C and V_{CE} .

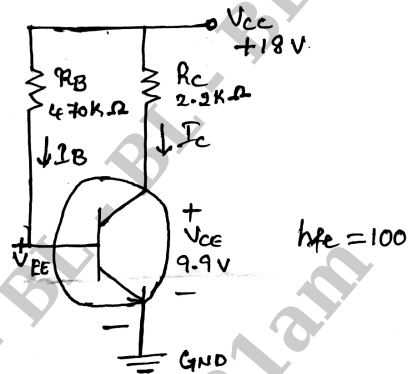


Fig Q1(c)

(06 Marks)

OR

- 2 a. Explain the operation adjustable voltage Regulator? List the advantages of adjustable voltage Regulator over fixed voltage regulator. (08 Marks)
- b. Difference between Active filter and Passive filter. (06 Marks)
- c. Sketch the 2-bit Flash ADC? The digital i/p for a 4-bit DAC is $D = 0111$. Calculate its o/p voltage. Take $V_{OFS} = 15$ V. (06 Marks)

Module-2

- 3 a. Prove De Morgan's theorem. (04 Marks)
- b. Simplify the following Boolean function using K-map method.
 $F(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 8, 9, 10, 11, 13, 14, 15)$ (06 Marks)
- c. Find all the prime impicates of the function using Q-M method.
 $f(a, b, c, d) = \sum m(0, 2, 3, 4, 8, 10, 12, 13, 14)$ (10 Marks)

OR

- 4 a. For the following function given use Q-M method and obtain essential prime impicates chart. $F(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$. (08 Marks)
- b. With an example, explain Petrick's method. (06 Marks)
- c. Explain Map –Entered variables method. (06 Marks)

Module-3

- 5 a. Realize $f(a, b, c, d) = \sum m(0, 3, 4, 5, 8, 9, 10, 14, 15)$, using three input NOR gates. (06 Marks)
- b. Discuss different types of hazards in combinational circuits. (08 Marks)
- c. With a neat diagram, explain 8 to 3 priority encoder. (06 Marks)

OR

- 6 a. Explain the programmable logic arrays (PLA).
Realize the following functions using PLA
 $f_1 = a'bd + abd + ab'c' + b'c$
 $f_2 = a'bd + c$
 $f_3 = abd + ab'c' + bc$ (10 Marks)
- b. Explain with the help of a logic diagram and truth table a 3 to 8 line decoder. (10 Marks)

Module-4

- 7 a. With a neat diagram, explain the VHDL program structure. (06 Marks)
- b. Discuss the switch debouncing with an SR latch. (06 Marks)
- c. Write the following Flip-flops characteristics equation and truth table.
 i) SR flip-flop ii) J-K flip-flop iii) D-Flip-flop iv) T-Flip-flop. (08 Marks)

OR

- 8 a. What is T Flip-Flop? Show how to convert JK Flip-Flop into T Flip-Flop. (08 Marks)
- b. Discuss the NAND-gate version of gated S-R latch. (06 Marks)
- c. Difference between Flip-Flop and Latch. (06 Marks)

Module-5

- 9 a. Define Counter. Describe the working of parallel adder with accumulator. (08 Marks)
- b. Discuss the working of a 3-bit shift register. (06 Marks)
- c. Difference between Synchronous and Asynchronous counters. (06 Marks)

OR

- 10 a. Explain the working of a 3-bit Binary Ripple Counter, waveforms and truth table. (06 Marks)
- b. What is the clock frequency of a 3 – bit ripple counter, if the period of the MSB waveform is $24\mu s$? (04 Marks)
- c. Design with a neat sketch and relevant expressions, explain a 3-bit binary up-down counter using D-Flip-Flop. (10 Marks)

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Third Semester B.E./B.Tech. Degree Examination, June/July 2025 Computer Organization and Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. With a neat diagram, analyze the basic operational concepts of a computer. Give the operating steps. (06 Marks)
 b. Explain the basic instruction types with examples. (04 Marks)
 c. Explain: (i) Processor clock
 (ii) Clock rate
 (iii) Basic performance equation
 (iv) Performance measurement (10 Marks)

OR

- 2 a. Define addressing mode, explain any three addressing modes with examples. (10 Marks)
 b. Write an assembly program that reads a line of characters and displays it. (06 Marks)
 c. Explain Big-Endian and Little-Endian addressability. (04 Marks)

Module-2

- 3 a. Define Interrupt. Explain various ways of enabling and disabling interrupts. (08 Marks)
 b. With a neat diagram, explain any three methods for handling multiple interrupt requests raised by multiple devices. (12 Marks)

OR

- 4 a. With a neat diagram, explain DMA. Briefly explain centralized bus arbitration technique. (10 Marks)
 b. Explain synchronous and Asynchronous bus with timing diagrams. (10 Marks)

Module-3

- 5 a. With a neat diagram, explain the internal organization of 128×8 memory chip. (10 Marks)
 b. What is cache memory? Explain the direct and associative mapping techniques. (10 Marks)

OR

- 6 a. What is memory interleaving? Explain with an example. (10 Marks)
 b. Define Virtual memory. Explain the address translation. (10 Marks)

Module-4

- 7 a. Draw 4-bit carry-look-ahead adder and explain. (10 Marks)
 b. Perform multiplication for +13 and –6 using Booth's algorithm. Explain Booth's algorithm. (10 Marks)

OR

- 8 a. Explain three-bus organization of data path with a neat diagram. (06 Marks)
 b. Explain Hard wired control unit organization in a processing unit. (06 Marks)
 c. Write actions required and control sequence for execution of instruction ADD (R3), R1. (08 Marks)

Module-5

- 9 a. Define Parallel Processing. Explain processor with multiple functional units. (10 Marks)
b. Define Pipelining. Explain five stage instruction pipeline with timing diagram. (10 Marks)

OR

- 10 a. Explain arithmetic pipeline with suitable example. (10 Marks)
b. Explain instruction pipeline with suitable example. (10 Marks)

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